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In re the Application of: **HAEMATSU, Hitoshi**

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For: **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF**

**SUBMISSION OF ENGLISH TRANSLATION OF JAPANESE APPLICATION**

Commissioner for Patents
P.O. Box 1450
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Sir:

A marked-up copy of the specification for the above-identified application was erroneously submitted with the Amendment filed on August 23, 2004. Enclosed please find an English translation of Japanese Patent Application 2001-165701 which was inadvertently omitted from the Amendment filed on August 23, 2004.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

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[Title of the invention] SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

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[Document] Specification 1

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[NAME OF DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION] SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

[WHAT IS CLAIMED IS:]

[CLAIM 1]

A semiconductor device, comprising:

a plurality of electrodes connected to an active region of a front face of a semiconductor chip;

a resin insulating film provided on the active region;

a metal protective film covering all of an upper surface and side surfaces of said resin insulating film; and

one or a plurality of electrical connecting portions of a reverse face leading out at least one electric potential of said plurality of electrodes, provided at the reverse face of the semiconductor chip.

[CLAIM 2]

The semiconductor device according to claim 1,

wherein all the electric potential of said plurality of electrodes are led out to the reverse face by said electrical connecting portion of the reverse face.

[CLAIM 3]

The semiconductor device according to claim 1,

wherein one of said plurality of electrodes is connected to said metal protective film.

[CLAIM 4]

The semiconductor device according to claim 1,

wherein a plurality of electrodes on the same electric potential of said plurality of electrodes are connected to said metal protective film.

[CLAIM 5]

The semiconductor device according to claim 1,

wherein said resin insulating film is provided above all of the front face of the semiconductor chip and said metal protective film covers the upper surface and the side surfaces of said resin insulating film.

[CLAIM 6]

The semiconductor device according to claim 1,

wherein said resin insulating film is provided above some part of the front face of the semiconductor substrate and said metal protective film covers the upper surface and the side surfaces of said resin insulating film.

[CLAIM 7]

The semiconductor device according to claim 6, further comprising:

an electrical connecting portion of the front face isolated electrically from said metal protective film on a region of the semiconductor chip where said resin insulating film is not provided,

wherein said electrical connecting portion of the front face is connected to said electrical connecting portion of the reverse face.

[CLAIM 8]

The semiconductor device according to any one of claims 1 to 7,

wherein connection between the front face and the reveres face of the semiconductor chip is performed via a connecting hole going through the semiconductor chip.

[CLAIM 9]

The semiconductor device according to any one of claims 1 to 7,

wherein connection between the front face and the reveres face of the semiconductor chip is performed through an electrical connecting portion of a side surface provided at the side surface of the semiconductor chip.

[CLAIM 10]

The semiconductor device according to any one of claims 1 to 9,

wherein the semiconductor chip is a compound semiconductor.

[CLAIM 11]

The semiconductor device according to claim 10,

wherein said plurality of electrodes comprise a gate electrode, a source electrode, and a drain electrode, and the active region composes a FET.

[CLAIM 12]

The semiconductor device according to claim 11,

wherein the source electrode is connected to said metal protective film, and the gate electrode and the drain electrode are connected to said respective electrical connecting portions of the reverse face.

[CLAIM 13]

The semiconductor device according to claim 11,

wherein the gate electrodes, the source electrodes, and the drain electrodes are plurally arranged in a shape of teeth of a comb, the source electrodes being connected to said metal protective film and the gate electrodes and the drain electrodes being connected to said respective electrical connecting portions of the reverse face.

[CLAIM 14]

The semiconductor device according to any one of claims 1 to 13,

wherein a foundation layer is formed between said metal protective film and said resin insulating film.

[CLAIM 15]

A semiconductor device wherein a front face of a semiconductor chip is protectively covered with a resin insulating film and all of said resin insulating film is covered with a metal protective film having moisture resistance.

[CLAIM 16]

The semiconductor device according to claim 15,

wherein said semiconductor chip is a compound semiconductor.

[CLAIM 17]

A manufacturing method of a semiconductor device, comprising the steps of:

a step of forming a plurality of electrodes on a front face of a semiconductor chip;

a step of covering the front face of the semiconductor chip with a resin insulating film;

a step of covering all of an upper surface and side surfaces of said resin insulating film with a metal protective film; and

a step of providing an electrical connecting portion of at least any of the plurality of electrodes at a reverse face of the semiconductor chip.

[CLAIM 18]

The manufacturing method of the semiconductor device according to claim 17,

wherein a metal layer is formed on a peripheral isolation region on the front face of the semiconductor chip when covering the side surface of the resin insulating film with the metal protective film.

[CLAIM 19]

The manufacturing method of the semiconductor device according to claim 17, further comprising the step of:

a step of exposing one of the plurality of electrodes from the upper surface of said resin insulating film to be connected to the metal protective film.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[FIELD OF THE INDUSTRIAL AVAILABILITY]

The present invention relates to a semiconductor device and a manufacturing method thereof, and more particularly, the present invention is best suited

when applied to a semiconductor device using a resin insulating film such as polyimide, BCB, or the like.

[0002]

[CONVENTIONAL ART]

Conventionally, a resin insulating film such as polyimide, BCB, or the like is generally used as a front face protective film for a chip mounted by mold etc.

[0003]

An example of a chip using an insulating film such as polyimide, BCB, or the like as a front face protective film is shown in Fig. 8. Fig. 8(A) and Fig. 8(B) are plane views showing a front face of the chip. Fig. 8(C) is a sectional view taken along the c-c line in Fig. 8(B). Fig. 8(D) is a sectional view taken along the d-d line in Fig. 8(B). Fig. 8(E) is a bottom view showing a reverse face of the chip.

[0004]

On an operating layer of a semiconductor substrate 101, a source electrode, a gate electrode and a drain electrode are formed in a shape of teeth of a comb. A source pad 102, a gate pad 103 and a drain pad 104 are respectively led out from the respective electrodes on the front face of the semiconductor substrate 101.

[0005]

The upper side of the operating layer of the semiconductor is covered with a surface protective insulating film 105 such as polyimide etc. A view in

Fig. 8(A) shows a specification in which only the upper side of the operating layer is covered with the surface protective insulating film 105. A view in Fig. 8(B) shows a specification in which all the regions except the respective pad areas 102 to 104 are covered with the surface protective insulating film 105. Thus, exposure of the electrodes and the semiconductor area on the front face of the chip is reduced so as to take a structure aiming for improvement of reliability.

[0006]

Generally on the chip as structured above, the source pad 102 is connected to a pad 102A on the reverse face of the chip through a via hole 102B, and the pad 102A on the reverse face is mounted as ground of the source.

[0007]

[PROBLEMS WHICH THE INVENTION IS TO SETTLE]

As described above, an insulating film such as polyimide, BCB, or the like is often used as a front face protective film of a conventional chip. However, a device using polyimide or BCB cannot be utilized for application which requires a high reliability. For example, polyimide has a high water absorbing property and would be saturated with absorbed water in the long term. Then, the water would be soaked out up to fingers such as the gate, the source, and the like to induce corrosion, ion migration, and so on. Therefore, there could be a risk of causing a device trouble. On

the other hand, BCB is said to have an extremely small water absorbing property. However, interface between metal and BCB, and BCB itself would be permeated with water. Therefore, there could be a risk of causing the aforementioned trouble.

[0008]

Due to the above-described problems related to moisture resistance, a highly airtight hermetic seal package is used for a device which requires higher reliability. However, a hermetic seal package is extremely expensive and in some cases it costs several times as much as a chip. Therefore, it will be a big barrier when trying to reduce costs of the product.

[0009]

The present invention is made in view of the aforementioned problems. Therefore, it is an object of the invention to obtain a highly reliable semiconductor device having a significantly improved moisture resistance while using an insulating film such as polyimide, BCB, or the like.

[0010]

[MEANS FOR SOLVING THE PROBLEMS]

The present invention is made in view of the aforementioned problems. Here, metal is focused on because it is easily available, is easily subjected to microfabrication, is a general material used in semiconductor manufacturing, and has a high moisture resistance. Therefore, metal is used to cover all of

an upper surface and side surfaces of polyimide, BCB, or the like which is applied as an insulating film above the front face of the semiconductor substrate. That is, in the semiconductor device according to the invention, the front face of a semiconductor chip is covered protectively with the insulating film as well as the whole surfaces of the aforementioned insulating film is covered with a metal protective film having moisture resistance.

[0011]

A problem when covering the insulating film with metal is that metal is conductive. It is needless to say that the chip cannot work when formed by a usual electrode forming method because all exposed electrodes and pads etc. will be short-circuit. Consequently, in this invention a structure is adopted so that all the necessary electrodes are led out from the front face to the reverse face. In other words, the semiconductor device according to this invention includes a plurality of electrodes connected to an active region on the front face of the semiconductor chip, a resin insulating film provided on the aforementioned active region, a metal protective film covering all of the upper surface and the side surfaces of the aforementioned resin insulating film, and one or a plurality of electrical connecting portions of the reverse face provided at the reverse side of the aforementioned semiconductor chip, leading out at least

one electric potential of the aforementioned plurality of electrodes to the reverse face.

[0012]

Additionally, a manufacturing method of a semiconductor device according to this invention includes a step of forming a plurality of electrodes on a front face of a semiconductor chip, a step of covering the front face of the aforementioned semiconductor chip with a resin insulating film, a step of covering all of the upper surface and the side surfaces of the aforementioned resin insulating film with a metal protective film, and a step of providing an electrical connecting portion of at least any of the aforementioned plurality of electrodes at the reverse face of the aforementioned semiconductor chip.

[0013]

[EMBODIMENT]

Embodiments of a semiconductor device and a manufacturing method thereof according to the present invention will be described hereinafter with reference to the drawings.

[0014]

-First Embodiment-

A chip of a first embodiment is shown in Fig. 1. Fig. 1(A) is a plane view showing a front face of the chip and Fig. 1(B) is a bottom view of a reverse face of the chip.

[0015]

On an operating layer (an active region) of a semiconductor substrate, a source electrode 11, a gate electrode 12 and a drain electrode 13 composing a FET are formed in a shape of teeth of a comb.

[0016]

A source via hole receiving pad 11A led out from the source electrode 11 is provided on the front face of the semiconductor substrate, while a source bonding pad 11B is provided on the reverse face. These source via hole receiving pad 11A and source bonding pad 11B are connected to each other through a via hole 11C. In other words, electric potential of the source electrode 11 is led out to the source bonding pad 11B on the reverse face.

[0017]

Similarly 12A is a gate via hole receiving pad on the front face of the semiconductor substrate led out from the gate electrode 12, 12B is a gate bonding pad on the reverse face, and 12C is a via hole. As well, 13A is a drain via hole receiving pad on the front face of the semiconductor substrate led out from the drain electrode 13, 13B is a drain bonding pad on the reverse face, and 13C is a via hole.

[0018]

In this embodiment all regions except a peripheral isolation region on the front face of the semiconductor substrate are covered with a resin insulating film 14 such as polyimide. That is, all the aforementioned

electrodes 11 to 13 and the via hole receiving pads 11A to 13A are covered with the insulating film 14.

[0019]

The upper surface of the aforementioned insulating film 14 is covered with a metal film 15. As a method of covering the insulating film 14 with the metal film 15, either one of sputtering, deposition, plating or combinations thereof may be used. It is noted that although the electrodes 11 to 13 and the via hole receiving pads 11A to 13A actually cannot be seen from the outside as they are covered with the insulating film 14 and the metal film 15, they are shown in Fig. 1(A) for the purpose of illustration.

[0020]

At the peripheral isolation region on the front face of the semiconductor substrate, a fringe metal layer 16 which strengthens adhesion to the semiconductor substrate is formed. A side surface of the aforementioned insulating film 14 is then covered with this fringe metal layer 16.

[0021]

As described above, the metal film 15 performs as an upper surface protective film of the insulating film 14, while the fringe metal layer 16 performs as a side surface protective film of the insulating film 14. Therefore, the chip is so structured that all of the upper surface and the side surfaces of the insulating film 14 are covered with the metal protective films.

Thereby, a significantly superior moisture resistance will be realized because exposed parts of both faces on the device are composed only of the semiconductor substrate or the metal which adheres strongly to this semiconductor substrate.

[0022]

Incidentally, when mounting the chip in the case of this embodiment, both faces will be turned upside down as compared with the usual case and it bonds to the respective bonding pads 11B to 13B of the source, the gate, and the drain on the reverse face of the chip.

[0023]

By adopting the structure that all of the upper surface and the side surfaces of the insulating film 14 are covered with the metal as described above, applied implementation as follows can be realized.

(1) By connecting one of a plurality of electrodes such as the source, the gate, and the drain to the metal protective film, the metal protective film can be utilized as an electrode.

(2) In a case that a certain electrode is connected to the metal protective film, if there are a plurality of these electrodes, for example if there are a plurality of the electrodes such as the source electrodes 11 shown in Fig. 1(A), those plurality of electrodes on the same electric potential (a plurality of the source electrodes 11) may be connected to the metal protective film.

(3) The metal protective film only needs to cover the upper surface and the side surfaces of the insulating film. Therefore, when there are some areas which are not covered with the insulating film above the front face of the chip, those uncovered regions need not be covered with the metal protective film.

(4) The electrode which is led out to the reverse face of the chip may be led out again to the front face of the chip within the "uncovered regions with the insulating film" described in (3).

(5) The connection between the front face and the reverse face of the chip may be performed by using the side surface of the chip in addition to using the via hole.

[0024]

These applied examples have the following effects. For example, in the applied examples (1) and (2), when the electrode which is connected to the metal protective film is ground electric potential such as ground etc., an electromagnetic shield effect by the metal protective film can be obtained. Since a plurality of the electrodes are connected to the metal protective film especially in the applied example (2), heat release occurs through the metal protective film having a large superficies. Therefore, the heat release property can be improved. Additionally, in the applied example (4) a contact above the front face of the chip will be possible.

[0025]

-Second Embodiment-

A second embodiment corresponds to the aforementioned applied examples (1) and (2). Specifically the source electrode is connected to the metal protective film. A chip of the second embodiment is shown in Fig. 2. Fig. 2(A) is a plane view showing a front face of the chip. Fig. 2(B) is a sectional view taken along the b-b line in Fig. 2(A). Fig. 2(C) is a sectional view taken along the c-c line in Fig. 2(A). Fig. 2(D) is a sectional view taken along the d-d line in Fig. 2(A). Fig. 2(E) is a bottom view of a reverse face of the chip.

[0026]

On an operating layer of a semiconductor substrate, a source electrode 21, a gate electrode 22, and a drain electrode 23 composing a FET are formed in a shape of teeth of a comb.

[0027]

A gate via hole receiving pad 22A led out from the gate electrode 22 is provided on the front face of the semiconductor substrate, while a gate bonding pad 22B is provided on the reverse face. These gate via hole receiving pad 22A and gate bonding pad 22B are connected to each other through a via hole 22C.

[0028]

Similarly a drain via hole receiving pad 23A led out from the drain electrode 23 is provided on the

front face of the semiconductor substrate, while a drain bonding pad 23B is provided on the reverse face. These drain via hole receiving pad 23A and drain bonding pad 23B are connected to each other through a via hole 23C.

[0029]

At a peripheral isolation region on the front face of the semiconductor substrate, a fringe metal layer 26 which strengthens adhesion to the semiconductor substrate by alloying is formed. This isolation region is isolated as a semiconductor and is electrically independent completely.

[0030]

Here, as shown in Fig. 2(B) and Fig. 2(C), the source electrode 21 is formed to be higher by wiring of the second layer than the gate electrode 22, the gate via hole receiving pad 22A and the drain electrode 23, the drain via hole receiving pad 23A, and is formed to approximately the same height as the fringe metal layer 26.

[0031]

Within the inner side of the fringe metal layer 26, polyimide etc. as an insulating film 24 is applied and the gate electrode 22, the drain electrode 23, the gate via hole receiving pad 22A and the drain via hole receiving pad 23A are covered with the insulating film 24. Therefore, different electrodes are insulated from

one another. However, only the source electrode 21 is exposed to the upper surface of the insulating film 24.

[0032]

Then, all of the upper surface of the insulating film 24, the upper surface of the fringe metal layer 26 and the upper surface of the source electrode 21 exposed to the upper surface of the insulating film 24 are covered with the metal film 25. Therefore, the source electrode 21 and the fringe metal layer 26 are connected through this metal film 25. However, the metal film 25 is insulated from the gate electrode 22 (the gate via hole receiving pad 22A) and the drain electrode 23 (the drain via hole receiving pad 23A) by the insulating film 24.

[0033]

It is noted that though the electrodes 21 to 23 and the via hole receiving pads 22A and 23A actually cannot been seen from the outside as they are covered with the metal film 25, they are shown in Fig. 2(A) for the purpose of illustration.

[0034]

As described above, the metal film 25 performs as an upper surface protective film of the insulating film 24 and the fringe metal layer 26 performs as a side surface protective film of the insulating film 24. Therefore, the chip is so structured that all of the upper surface and the side surfaces of the insulating film 24 are covered with the metal protective films and

a significantly superior moisture resistance can be realized. Moreover, since there is no need to lead out the source electrode 21 to the reverse face of the semiconductor substrate, the source via hole receiving pad and the source bonding pad described in the first embodiment will not be needed. Therefore, similarly to the chip having the source via hole structure described in the conventional example, it becomes possible to mount the chip by utilizing the reverse face to the bonding face of the gate and the drain (that is, the face with the metal protective film) as ground of the source. In addition, since the metal film 25 above the front face of the chip can be flattened, it becomes possible to mount the chip easily on the device where the main way of mounting is flip chip mounting.

[0035]

Referring to Fig. 2 to Fig. 5, a method of manufacturing the semiconductor device according to this embodiment will be explained hereinafter. Here, it will be explained by taking MESFET for instance, which is a compound semiconductor device using a GaAs substrate etc. and has a high-frequency characteristic. Note that the same components as described in Fig. 2 will be explained with the same reference numerals and symbols in Fig. 3 to Fig. 5.

[0036]

First of all, isolation is performed to the semiconductor substrate 27 by a method such as ion

implantation, mesa etch, or the like so as to form an operating layer 30.

Subsequently as shown in Fig. 3, a gate electrode 22 subjected to Schottky junction using metal such as WSi etc., and a source electrode 21 and a drain electrode 23 with an ohmic property using metal such as AuGe etc., are formed in a shape of teeth of a comb on the operating layer 30. An Au-plating layer with a film thickness of about 3 $\mu$m is formed for the ohmic metal to secure electric current density of the electrode.

[0037]

Furthermore, a gate via hole receiving pad 22A and a drain via hole receiving pad 23A are provided on the front face of the semiconductor substrate 27. Then, a fringe metal layer 26 is formed on the isolation region outside the operating layer 30.

[0038]

Thereafter, polyimide as the insulating film 24 is applied to whole surfaces as shown in Fig. 4. Then, opening portions 28 are formed at the source electrode 21-1 and the fringe metal layer 26-1 of the insulating film 24 to expose the upper surfaces of these source electrode 21-1 and fringe metal layer 26-1. As a process of making the openings, etching etc. with chemicals using a photosensitive polyimide as the insulating film 24 may be performed.

[0039]

A source wiring 21-2 of the second layer and a fringe metal layer 26-2 of the second layer are then formed at the opening portions 28 by electrolytic Au plating as shown in Fig. 5. In other words, after forming the opening portions 28, metal is deposited on the whole surfaces by a method such as sputtering, and then patterning is performed to make smaller areas than the opening portions 28 for plating. Subsequently the Au-plating layer with a film thickness of about 4 $\mu$m is formed. By using this Au-plating layer as a mask, the metal which is deposited by a method such as sputtering should be removed by etching such as milling method.

[0040]

Next polyimide as the insulating film 24 is applied to the whole surfaces as shown in Fig. 6. Then, opening portions 29 are formed at the source electrode 21-2 (the source wiring of the second layer) and the fringe metal layer 26-2 to expose the upper surfaces of these source electrode 21-2 and fringe metal layer 26-2. At this time as shown in Fig. 6(B), only the upper surface of the source electrode 21-2 (the source wiring of the second layer) is exposed to the front face of the chip inside the fringe metal layer 26-2, while other electrodes 22, 23 and pads 22A, 23A are covered with the insulating film 24.

[0041]

Thereafter, metal such as Ti or Ni etc. are deposited on the whole surfaces by a method such as sputtering. Then, patterning is performed with resist so as to make a rectangular opening slightly inside of the chip region (inside of the outer edge of the fringe metal layer 26) above the transistor region which includes the fringe metal layer 26 and the gate electrode 21. Subsequently, an Au-plating layer with a film thickness of about 3 $\mu$m is formed and the resist is removed. As described above the metal film 25 is formed as shown in Fig. 2(B) to complete the forming step of the front face of the substrate. The metal film 25 composing the metal protective film has a foundation layer of the sputtered metal and the Au-plating layer, so that adhesiveness to the insulating film 24 can be increased.

[0042]

Next, proceeding to the forming step of the reverse face of the substrate, the via holes 22C and 23C are formed from the reverse face of the semiconductor substrate 27 by dry etching etc. as shown in Fig. 2(C) and Fig. 2(E). Then, respective bonding pads 22B and 23B are plated with Au to complete the chip according to this embodiment.

[0043]

-Third Embodiment-

A third embodiment corresponds to the aforementioned applied example (4). In Fig. 7, a

chip of the third embodiment is shown. Fig. 7(A) is a plane view showing a front face of the chip and Fig. 7(B) is a bottom view showing a reverse face of the chip. It is noted that the difference from the second embodiment described above will be focused on hereinafter.

[0044]

Similarly to the second embodiment described above, a source electrode 31, a gate electrode 32, and a drain electrode 33 composing a FET are formed in a shape of teeth of a comb on an operating layer of a semiconductor substrate.

[0045]

A gate via hole receiving pad 32A led out from the gate electrode 32 is provided on the front face of the semiconductor substrate, while a pad 32B (which is referred to as "a gate relay pad" hereinafter) is provided on the reverse face. These gate via hole receiving pad 32A and gate relay pad 32B are connected to each other through a via hole 32C.

[0046]

Similarly, a drain via hole receiving pad 33A led out from the drain electrode 33 is provided on the front face of the semiconductor substrate, while a pad 33B (which is referred to as "a drain relay pad" hereinafter) is provided on the reverse face. These drain via hole receiving pad 33A and drain relay pad 33B are connected to each other through a via hole 33C.

[0047]

Similarly to the second embodiment described above, within the inner side of a fringe metal layer 36, polyimide etc. as an insulating film 34 is applied, and the gate electrode 32, the drain electrode 33, the gate via hole receiving pad 32A and the drain via hole receiving pad 33A are covered with the insulating film 34. Then, all of the upper surface of the insulating film 34, the upper surface of the fringe metal layer 36 and the upper surface of the source electrode 31 exposed to the upper surface of the insulating film 34 are covered with the metal film 35. Therefore, the source electrode 31 and the fringe metal layer 36 are connected to each other through this metal film 35.

[0048]

Here, as shown in Fig. 7(A), a peripheral isolation region on the front face of the semiconductor substrate is secured largely and space exists outside of the fringe metal layer 36 in this embodiment. In this space of the isolation region a gate bonding pad 32D is provided on the side of the gate via hole receiving pad 32A. This gate bonding pad 32D is connected to the gate relay pad 32B on the reverse face of the semiconductor substrate through another via hole 32E than the aforementioned via hole 32C. In other words, the gate electrode 32 is connected to the gate relay pad 32B on the reverse face through the via hole 32C further through the gate via hole receiving pad 32A

on the front face of the chip. Furthermore, it is connected to the gate bonding pad 32D on the front face through the via hole 32E.

[0049]

Similarly, in the space of the isolation region a drain bonding pad 33D is provided on the side of the drain via hole receiving pad 33A. This drain bonding pad 33D is connected to the drain relay pad 33B on the reverse face of the semiconductor substrate through another via hole 33E than the aforementioned via hole 33C. In other words, the drain electrode 33 is connected to the drain relay pad 33B on the reverse face through the via hole 33C further through the drain via hole receiving pad 33A on the front face of the chip. Furthermore, it is connected to the drain bonding pad 33D on the front face through the via hole 33E.

[0050]

Additionally, both sides of the fringe metal layer 36 are made larger in this embodiment as shown in Fig. 7(A) to be used as source electrode pads 31D.

[0051]

As described above, the metal film 35 performs as an upper surface protective film of the insulating film 34 and the fringe metal layer 36 performs as a side surface protective film of the insulating film 34. Therefore, the chip is so structured that all of the upper surface and the side surfaces of the insulating

film 34 are covered with the metal protective films. Thereby, a significantly superior moisture resistance will be realized. Moreover, bonding can be performed on both sides of the chip, so that mounting design with extremely high flexibility can be available.

[0052]

In the aforementioned first to third embodiments the insulating films 14, 24, and 34 are covered with the metal films 15, 25, and 35 as the upper surface protective films, as well as they are covered with the fringe metal layer 16, 26, and 36 as the side surface protective films. Thereby strengthened metal protective films are formed. However depending on required reliability, after forming an insulating film, metal may be formed on the whole surfaces of the insulating film at a time by sputtering, deposition, or the like without dividing the metal protective films into the upper part and the side part. Of course it can be considered that strength may be increased by Au-plating or the like on the once formed metal protective film. In this case, when the metal protective film which covers the resin insulating film terminates directly at a semiconductor substrate, an insulating film such as an $SiO_2$ film and an SiN film, or the like, reliability can be improved together with higher adhesiveness by using a foundation such as Ti, Ni, or the like, which has a superior adhesiveness.

[0053]

Incidentally, while the front face and the reverse face of the chip are connected through the via hole in the aforementioned first to third embodiments, it can be considered that this connection is realized by using a side face of the chip. For example, an electrical connecting member may be provided at the side face of the semiconductor chip so as to connect the front face and the reverse face of the aforementioned semiconductor substrate through this electrical connecting member.

[0054]

[EFFECT]

According to the present invention, in addition that the front face of the semiconductor chip is covered with the resin insulating film, this resin insulating film is further covered with the metal film. Thus, moisture resistance can be significantly improved to obtain a highly reliable semiconductor device without cost increase.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1]

Schematic views showing a chip of a first embodiment.

[FIG. 2]

Schematic views showing a chip of a second embodiment.

[FIG. 3]

A plane view illustrating a process of manufacturing the chip of the second embodiment.

[FIG. 4]

A sectional view illustrating a process of manufacturing the chip of the second embodiment.

[FIG. 5]

A sectional view illustrating a process of manufacturing the chip of the second embodiment.

[FIG. 6]

Schematic views illustrating a process of manufacturing the chip of the second embodiment.

[FIG. 7]

Schematic views showing a chip of a third embodiment.

[FIG. 8]

Schematic views showing a chip of a conventional example.

[EXPLANETION OF CODES]

11,21,31 source electrode

12,22,32 gate electrode

13,23,33 drain electrode

11A source via hole receiving pad

12A,22A,32A gate via hole receiving pad

13A,23A,33A drain via hole receiving pad

11B source bonding pad

12B,22B gate bonding pad

13B,23B drain bonding pad

32B a gate relay pad

33B drain relay pad

11C,12C,13C via hole

21C,22C,23C via hole

31C,32C,33C via hole

32D gate bonding pad

33D drain bonding pad

32E,33E via hole

14,24,34 insulating film

15,25,35 metal film

16,26,36 fringe metal layer

27 semiconductor substrate

28 opening portion

FIG. 1

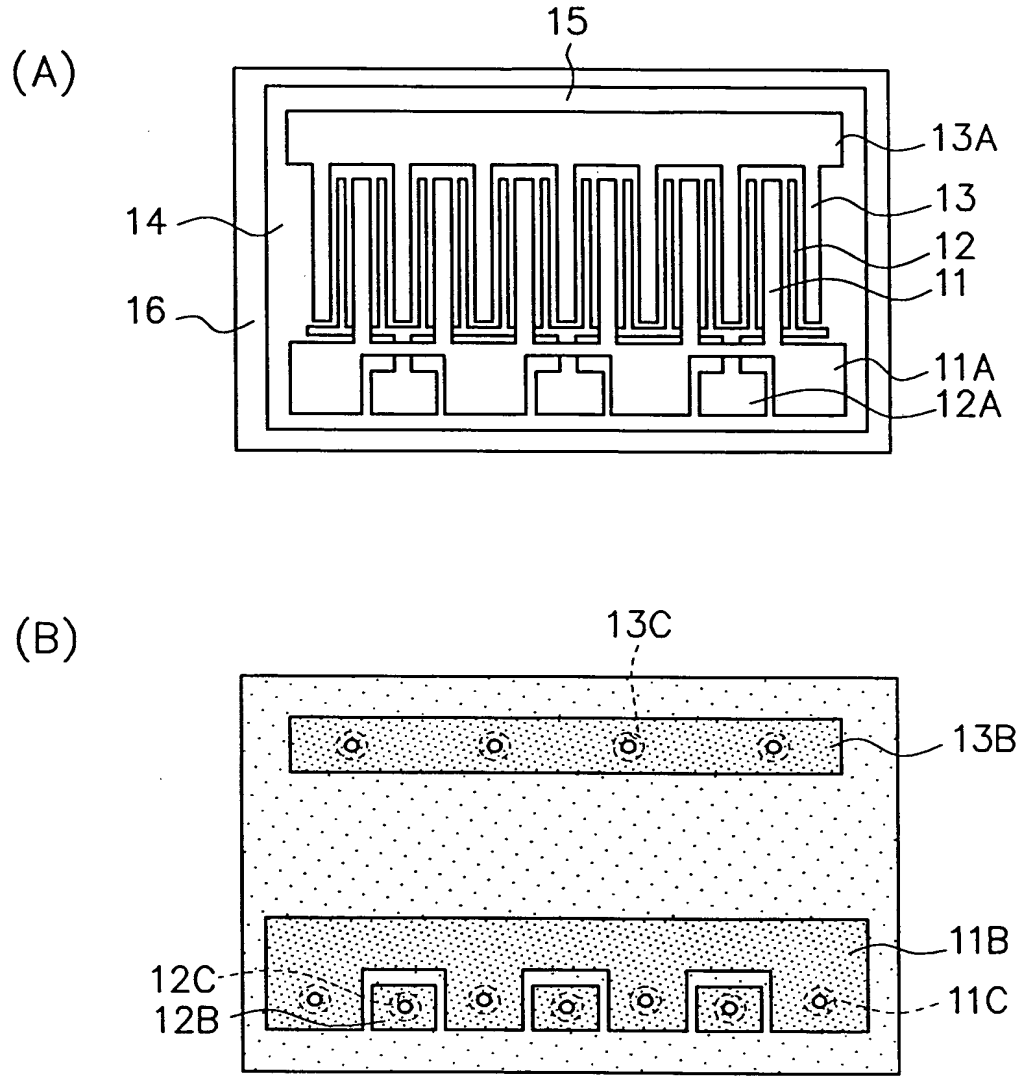


FIG. 2

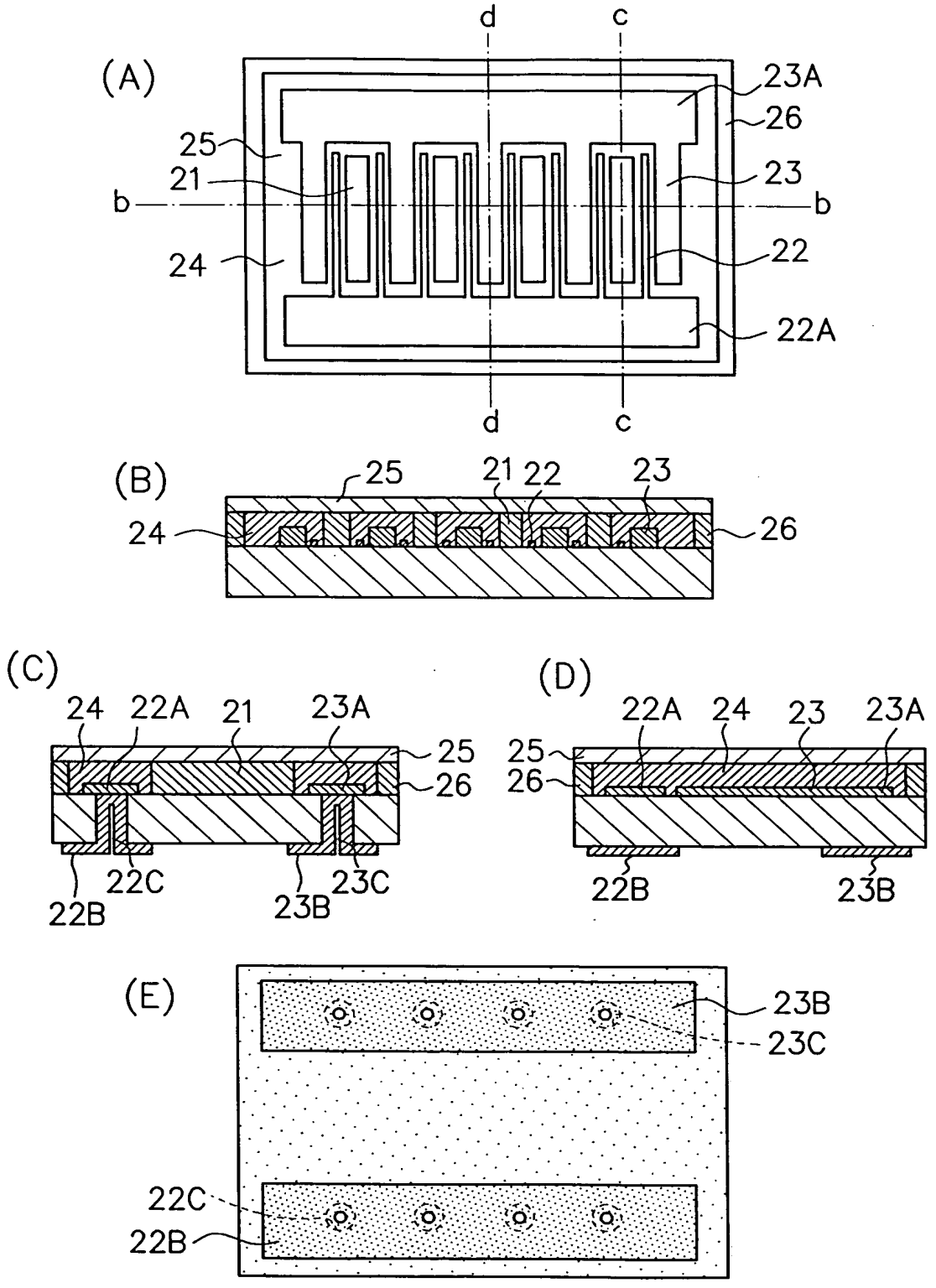

(A)
d
c
23A
26
25
21
23
b
b
24
22
22A
d
c
(B)
25
21
22
23
24
26
(C)
24
22A
21
23A
25
26
22C
23C
22B
23B
(D)
22A
24
23
23A
25
26
22B
23B
(E)
23B
23C
22C
22B

FIG. 3

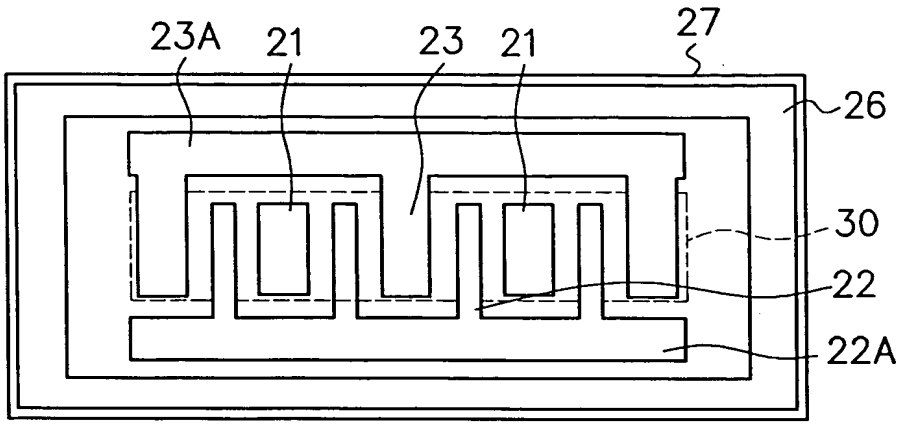



FIG. 4

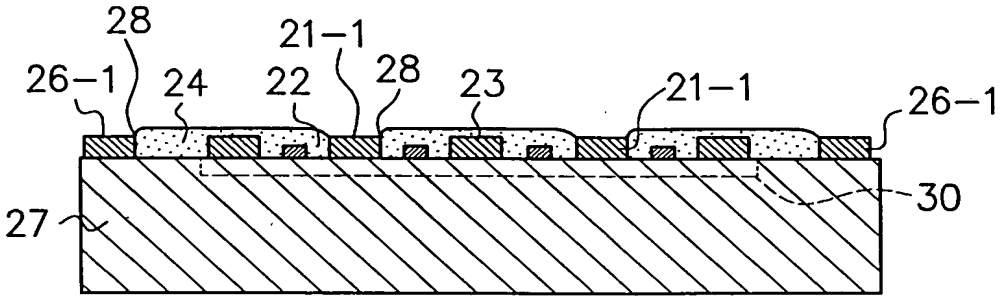


FIG. 5

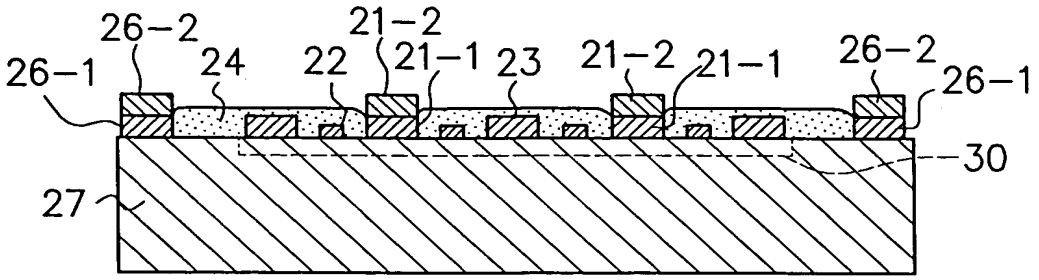

26−2
21−2
26−1
24
22
21−1
23
21−2
21−1
26−2
26−1
30
27

FIG. 6

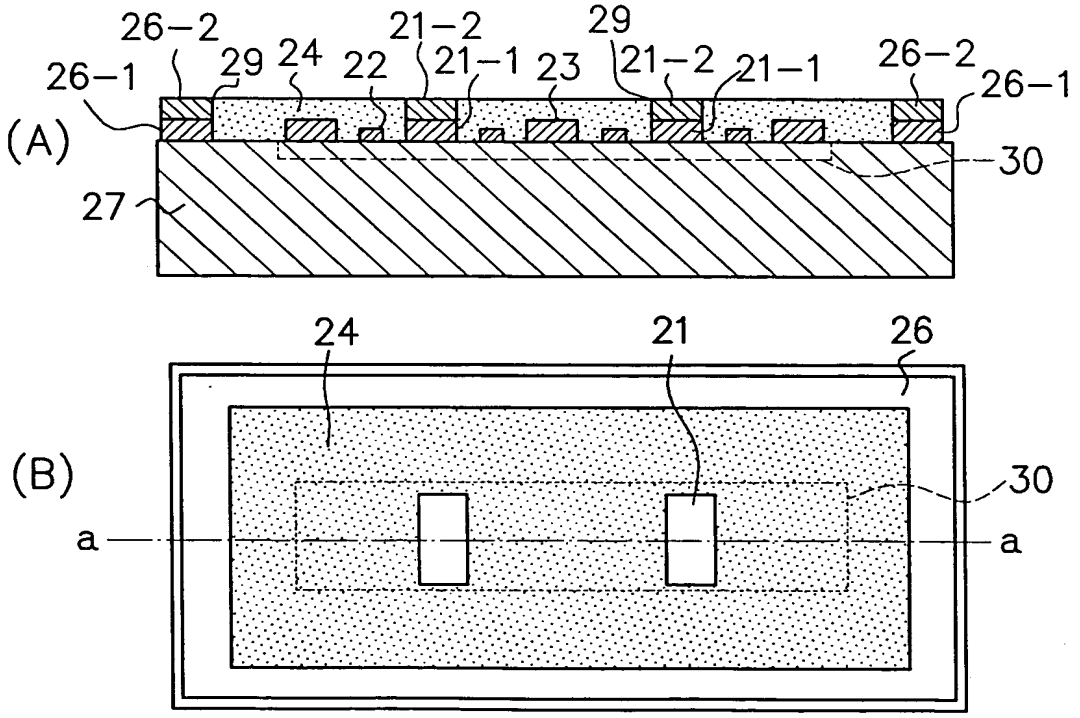

26−2
21−2
29
26−1
29
24
22
21−1
23
21−2
21−1
26−2
26−1
(A)
30
27
24
21
26
(B)
30
a
a

FIG. 7

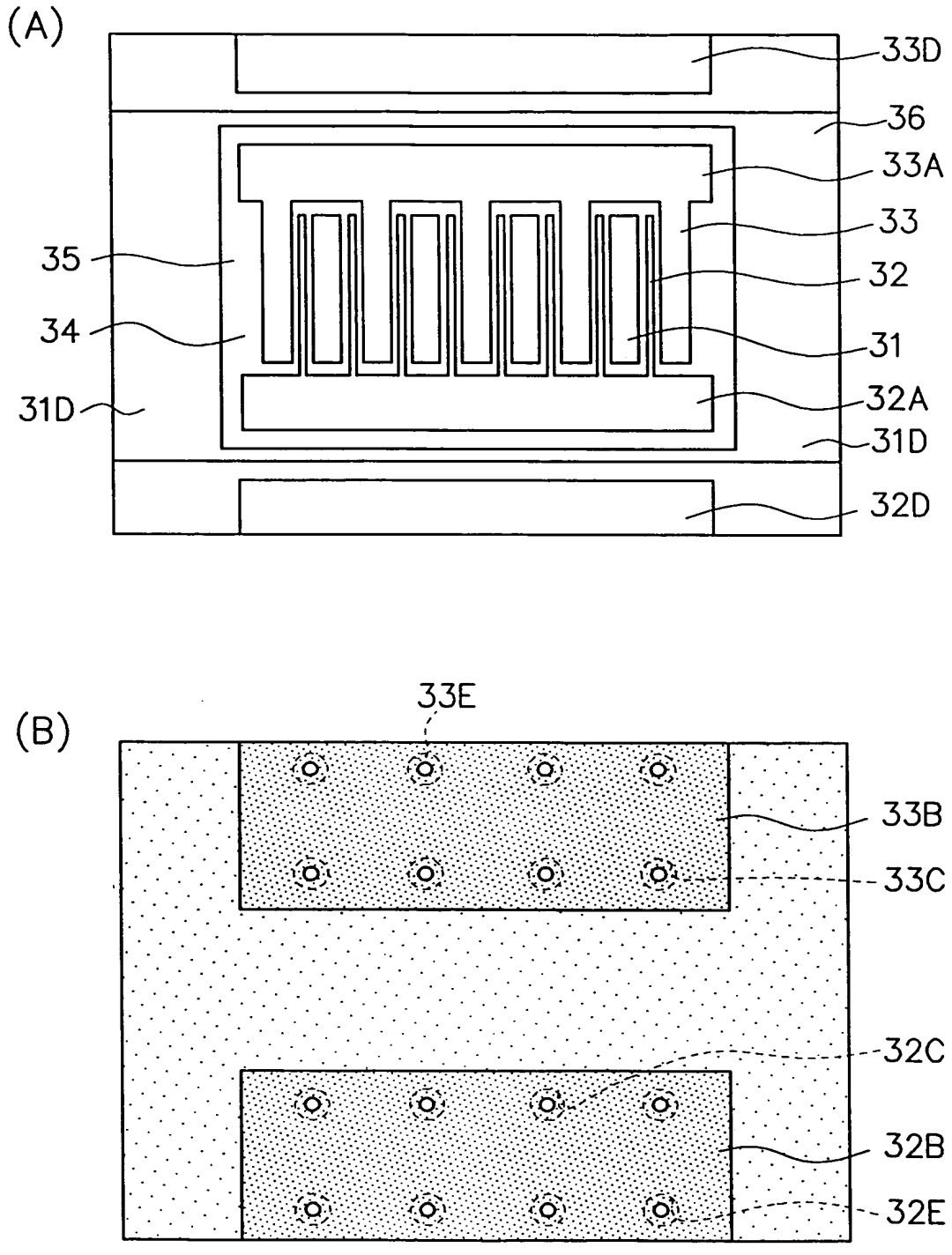
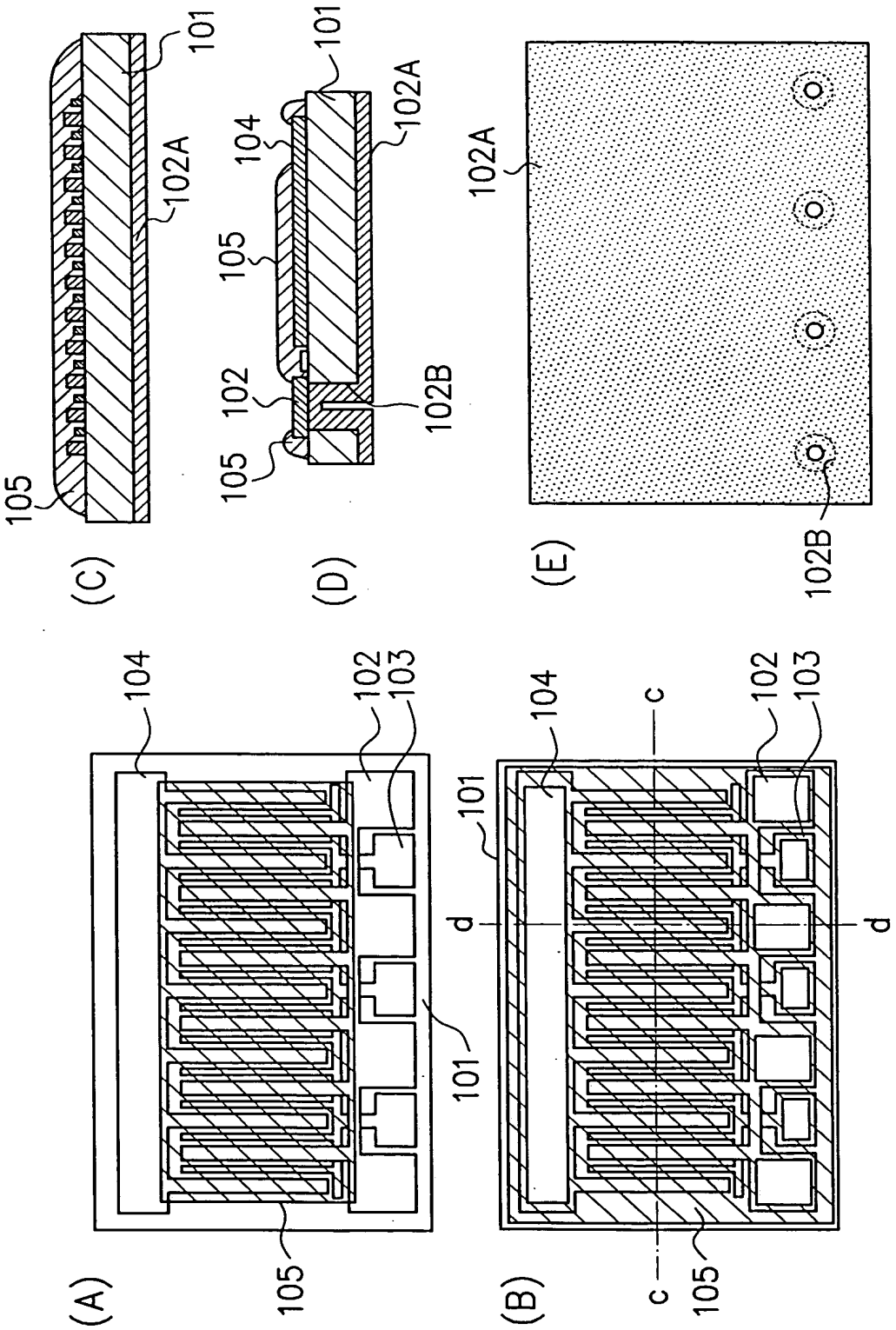

(A)
33D
36
33A
33
35
32
34
31
32A
31D
31D
32D
(B)
33E
33B
33C
32C
32B
32E

FIG. 8


(A)
104
102
103
105
(B)
104
101
c
102
103
d
d
101
c
105
(C)
101
102A
105
(D)
101
102A
104
105
102
102B
105
(E)
102A
102B

[NAME OF DOCUMENT] ABSTRACT

[SUMMARY]

[PROBLEM TO BE SOLVED] To obtain a highly reliable semiconductor device having a significantly improved moisture resistance.

[SOLUTION] A source electrode 11, a gate electrode 12, and a drain electrode 13 formed on a front face active region of a semiconductor substrate in a shape of teeth of a comb are covered with an insulating film 14 such as polyimede etc., as well as all of the upper surface and the side surfaces of the insulating film 14 are covered with a metal protective film 15, 16. Via hole receiving pads 11A, 12A, 13A connected to the source electrode 11, the gate electrode 12, and the drain electrode 13 are respectively connected to bonding pads 11B, 12B, 13B on a reveres face of the semiconductor substrate through via holes.

[SELECTED DRAWING] Fig. 1

# DECLARATION

I, Aya FUKUDA, of KOKUBUN International Patents & Trademarks of Ikebukuro TG Homest Building, 17-8, Higashi-Ikebukuro 1-chome, Toshima-ku, Tokyo 170-0013 JAPAN, hereby declare that I am well acquainted with both the Japanese and English languages, that I made an English translation attached hereto, and that to the best of my knowledge and belief the translation is a true and correct reproduction of the original documents filed with the Japanese Patent Office in respect of Japanese Patent Application No. 2001-165701 on May 31, 2001.

Signed this 12th day of August, 2004

Aya Fukuda

Aya FUKUDA